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(54) [Inventions name] INTERFACE CIRCUIT AND PHASE LOCKED LOOP USED THEREFORE

[57] [Abstract]

[Purpose]

To ensure the start-up of an interface circuit by preventing an oscillating frequency of the phase locked loop from being fixed at a frequency different from the frequency of a transmission signal.

[Structure]

A PLL control circuit 15 measures a period when a lock detection section 14 detects the synchronization between a transmission signal DIN and a basic clock BCK and when a specific period elapses in the process of measurement, a phase comparator 11 of the phase locked loop 10 and a voltage controlled oscillator 13 are reset. Since the reset phase locked loop 10 controls the oscillation of the voltage controlled oscillator 13 so that the basic clock BCK is synchronized with the transmission signal DIN, the starting of the phase locked loop is ensured.

[Patent application field]

[Application paragraph 1] Having the transmission signal of the fixed format sent from the transmission part device being received by the receiver part device, and this transmission signal being demodulated to the format correspondent to the mentioned receiver part device together with the basic clock synchronized with the transmission signal, the interface circuit provides the receiving means generating the clock 1 related to the timing of the switch of the bit by receiving the mentioned transmission signal, the phase locked loop means providing the control for the oscillation frequency of the voltage control oscillator in accordance to the phase difference also providing the phase comparing of clock 2 with the oscillation provided by the voltage

control oscillator with the mentioned clock 1, the demodulating means providing the demodulation of the mentioned transmission signal to the format correspondent to the mentioned receiver part device on the basis of clock 2, and the measurement means providing the measurement of the period before the clock number 2 were synchronized to the transmission signal from the transmission signal by the receiving means, and also provides the initial settings of the voltage control oscillation device when the value is united with the phase lock group during the measurement value being united.

[Application paragraph 2]

The interface circuit indicated within paragraph 1, determines an error within the demodulation signal demodulated by the mentioned demodulation means, or determines that the lock 2 was synchronized to the mentioned transmission signal, when there were no errors within the specific periods.

[Application paragraph 3]

The interface circuit indicated within the paragraph 1 determines that the clock 2 was synchronized to the mentioned transmission signal, when the phase comparing output was set within the fixed level field.

[Application paragraph 4]

Phase locked loop provides the voltage control oscillator generating the frequency clock correspondent to the respective control voltage, phase comparator comparing the phase of the clock oscillated within the voltage control oscillator and of the clock having fixed frequency, the low pass filter correspondent to the control voltage within the mentioned voltage control oscillation device by receiving the comparing output of the mentioned phase comparator , the measurement means providing

the measurement of the time period from the phase comparator and the voltage control oscillator start-up up to the synchronization of the clock oscillated within the voltage control oscillator to the standard clock; and provides the repeated initial measurement of the mentioned voltage control oscillator and the phase comparator during the measurement value being united in the process of measurement of the period from the measurement means start-up up to the synchronization of the clock 2.

[Inventions detailed explanation]

[0001]

[Technical application field] The titled invention corresponds to the interface circuit receiving the transmission signal by the receiver part in case when the transmission of the data between the multiple devices is provided.

[0002]

Conventional technique] The conventional structure, within the compact disk player and digital audio decoder and other digital audio devices, in case of the receiver part of the transmission signal, is composed in order to synchronize the received transmission signal, along with the demodulating of the received transmission signal to the respective format. Due to this structure, even in case of the format difference, the data relative cross is possible.

[0003]

The interface circuit receiving the transmission signal within the receiver part device is indicated in graph 5. The transmission signal Din sent from the sending part device is moved to the receiver circuit 1, inputted to the demodulation circuit 2 from the receiver circuit 1. The transmission signal Din, for example in reference to the EIAJ (Japan Electric Instrument Association), is

composed by the data part of the 4 bit fixed signal section and 28-bit data section, while the 32 bit signal is connected. In the receiver circuit 1, the switching of the data section bit of the transmission signal Din modulated within the by-phase signal, while the clock DCK referred to the switching timing is taken. This clock DCK is inputted to the phase lock loop 3, in order to have the basic clock BCK performing. The phase lock loop 3 is composed of the voltage control oscillator, phase comparison and has the output of the voltage control oscillator controlling the oscillation frequency in response to the phase comparator output, and provides the supply of the standard clock. Moreover, the demodulation circuit 2, being based on the fixed basic BCK clock synchronized with the transmission signal Din, has the demodulation processing provided towards the format correspondent to the parity check of each bit in response to the transmission signal, and has the output of the Audio Signal ADS in order to each circuit.

[0004]

On contrary, the sending part equipment is having the structure providing the sending to the transmission line after being demodulated to the common standard format from the format correspondent to the audio and up to the big format. Consequently, due to the interface circuit, within the receiver part device, the synchronizing to the transmission signal Din, and, due to that the audio signal ADS of the format are received, even in case of the audio device signal format is different.

[0005]

[Problems to be solved by the titled invention]

In the mentioned digital audio interface circuit the field having wide frequency of the transmission signal Din, in case of the

previous format EISJ, switching is provided to the 32-48 Kg, the synchronization is provided to the phase lock by the switch time of the frequency. In such case, within the phase lock loop, the phase comparator output is having the fixed time of the repatriation circuit returning the phase comparator output to the voltage control oscillator being low and the phase lock loop start-up being high, thus enabling the interface circuit to switch the frequency of the transmission signal D18.

[0006]

However, when the fixed number of the repatriation circuit of the phase lock loop 3 being low, the oscillation of the voltage control oscillator is becoming unstable, and the jitter within the basic clock BCK received from the phase lock loop is generated. Due to this, it is not possible to get the time fixed value of the repatriation circuit to the desired low level, so, in case of the frequency of the transmission signal Din being changed to high level, the basic clock BCK need long period of time to be synchronized with the transmission signal Din. Dependent on the case, when the 1 clock pulse of the basic clock BCK by chance is united with the clock DCK, the basic clock BCK frequency is set at the value different from the transmission signal Din, thus the phase lock loop could not be locked.

[0007]

In such situation, the titled invention, when the transmission signal frequency is changed, prevents the state when the phase lock loop could not be locked, and is oriented to prevent the state when the transmission signal receiving could not be provided.

[0008]

The titled invention taking to account the problem mentioned in above, is having the transmission signal of the fixed format sent

from the transmission part device being received by the receiver part device, and this transmission signal being demodulated to the format correspondent to the mentioned receiver part device together with the basic clock synchronized with the transmission signal, the interface circuit provides the receiving means generating the clock 1 related to the timing of the switch of the bit by receiving the mentioned transmission signal, the phase locked loop means providing the control for the oscillation frequency of the voltage control oscillator in accordance to the phase difference also providing the phase comparing of clock 2 with the oscillation provided by the voltage control oscillator with the mentioned clock 1, the demodulating means providing the demodulation of the mentioned transmission signal to the format correspondent to the mentioned receiver part device on the basis of clock 2, and the measurement means providing the measurement of the period before the clock number 2 were synchronized to the transmission signal from the transmission signal by the receiving means, and also provides the initial settings of the voltage control oscillation device when the value is united with the phase lock group during the measurement value being united at the process of measurement of the period from the measurement means start-up up to the synchronization of the clock 2.

[0009]

[Usage] Due to the titled invention, when the clock 2 oscillated within the voltage control oscillator of the phase lock loop is not synchronized with the clock 1 even when the specific period is elapsed, the phase comparator and voltage control oscillator are set to launch, and the clock 2 is having the frequency of the clock 2 compared by phase with the clock 1 being adjusted.

[0010]

[Practical example] The practical example of the titled invention is explained in the graph. The interface circuit structure of the titled invention is indicated within the graph 1. Due to this graph, the receiving circuit 1 and demodulation circuit 2, equally as in graph 5, are having the transmission signal Din sent from the transmission part device taken to the receiver circuit 1, and structured in order to provide the transmission signal Din from the receiver circuit 1 to the demodulation circuit 2.

[0011]

The titled invention is having the feature of re-set provided in case when the basic clock BCK is not synchronized with the transmission signal Din, even when the specific period is elapsed after having the transmission signal Din received by the receiving circuit 1. Consequently, the phase lock loop 10 consisting from the phase comparator 11 comparing the phase of the clock DCK and the basic clock BCK, and of the voltage control oscillator changing the oscillation frequency due to the control voltage Vc outputted by the low pass filter 12 or the low pass filter 12 receiving the output PD of the phase comparator 11, and when it is detected that the phase lock loop 10 is locked within the specific period, the phase comparator and voltage control oscillator are provided in such a way to launch the phase comparison of the basic clock BCK with the clock DCK after being reset.

[0012]

In the demodulation circuit, the lock detection section 14 is provided in order to detect the lock of the phase lock loop by means of the determination of whether the demodulation process was successfully provided, and has the period up to the moment when the phase locked loop 10 is locked measured by the PLL

measurement circuit 15 based on the lock detection section output LD. The loop detection part 11 is provided in such way to determine that the phase locked loop was locked, after the continuous parity check effect provided by the demodulation circuit 2, in case when the error did not occur. This enables to prevent of the errors occurred within the lock determination of the phase lock loop 10, and not to provide the determination if the phase lock loop was not locked, in case when the clock 1 pulse of the basic clock BCK was by chance united with the clock DCK.

[0013]

Moreover, the PLL control circuit 15, as it is indicated within the graph 2, being composed of the counter 16 providing the count-up within the basic BCK clock reset by the output LD of the lock detection section 14, and the decoder 17 providing the determination of whether the specific value was increased by the output of the counter 16, and is provided in order to count the basic clock BCK by the counter 16 up to the moment when the lock of the phase lock loop is detected by the lock detection section 14. Then, when the specific value is increased by the count value of the counter 16, and after the lock period of the specific clock is elapsed, the decoder 17 provides the reset pulse RSP to the phase comparator and voltage control oscillator of the phase lock loop 10. Consequently, when the lock of the phase lock loop 10 could not be confirmed even in case when the period correspondent to the value set in the decoder is elapsed, the phase lock loop 10 is initially set, and the phase control towards the transmission signal Din of the basic clock is newly provided.

[0014]

Due to the structure mentioned in above, even when the basic clock BCK is not synchronized to the transmission signal Din, the

phase lock loop 10 is reset within the time point when the specific period is elapsed, and the basic clock BCK clock 1 pulse being united by chance with the DCK while the basic clock is prevented from being fixed at the frequency different from transmission signal. Moreover, the method of the determination of the lock of the phase lock loop, being different from the method detecting the parity check error within the demodulation circuit 2, could also use the method of determination from the output from the low pass filter 13. For example, the output level of the low pass filter 13 is having the level determination circuit providing the determination of the control voltage Vc, thus being composed in order to provide the determination of whether the lock of the phase lock loop was provided when the control voltage Vc entered the fixed field. Moreover, the start-up or the end-up of the output PD of the phase comparator 11 could be determined, thus it is possible to provide the structure in order to determine the lock of the phase lock loop 10 measuring the period outputting the ground potential or the electric potential from the phase comparator 11.

[0015]

[Results of the titled invention] Due to the titled invention, it is possible to ensure the start-up of an interface circuit by preventing an oscillating frequency of the phase locked loop from being fixed at a frequency different from the frequency of a transmission signal, thus improving the effectiveness and credibility of the invention.

[Graph brief explanation]

[Graph 1] Block graph indicating the first practical example of the titled invention

[Graph 2] Circuit graph indicating the PLL control circuit.

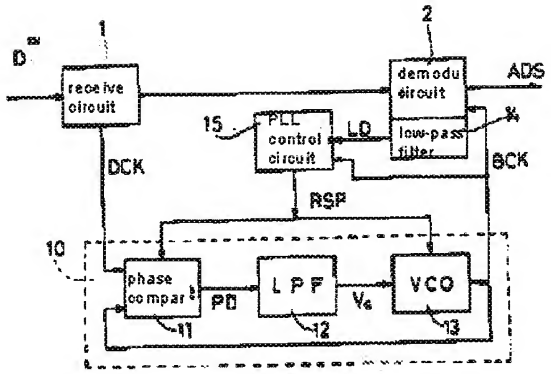
[Graph 3] Block graph indicating the conventional example of the interface circuit.

[Graph 4] Graph indicating the transmission signal format.

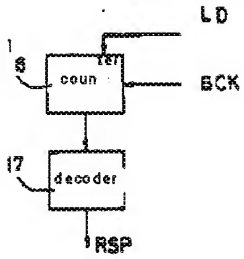
[Coding within graphs]

1. Receiving circuit
2. Demodulating circuit
3. 10. Phase lock loop
11. Phase comparator
12. Low pass filter
13. Voltage control oscillator
14. Lock detection section.
15. PLL control circuit
16. Counter
17. Decoder

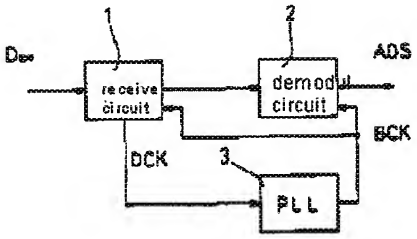
graph 1



graph 2



graph 3



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